Abstracts

Full wave analysis of electromagnetic coupling in realistic RF multilayer PCB layouts using cascaded parallel plate waveguide model

M.R. Abdul-Gaffoor, H.K. Smith, A.A. Kishk and A.W. Glisson. "Full wave analysis of electromagnetic coupling in realistic RF multilayer PCB layouts using cascaded parallel plate waveguide model." 2001 MTT-S International Microwave Symposium Digest 01.3 (2001 Vol. III [MWSYM]): 1933-1936 vol.3.

Realistic multilayer Printed Circuit Boards (PCBs) used in RF applications have large amount of metalization and a number of vias to provide good shielding and connectivity between nets in different layers. Taking advantage of these physical properties and using the equivalence principle, the multilayer PCB is modeled as a cascade of parallel plate waveguides with half-space regions residing above and below the PCB. Instead of formulating the problem in terms of electric currents in the horizontal metal layers, it is formulated using equivalent magnetic currents in the non-metallic regions of layer interfaces. The equivalent magnetic currents at the dielectric interfaces are expressed In terms of the Rao-Wilton-Glisson (RWG) basis functions. The electric currents flowing on the vias inside dielectric layers are assumed constant in the vertical direction. These vertical electric currents radiate TEM modes in the parallel plate environment. Integral equations based on simple parallel plate and free-space Green's functions enforcing the boundary conditions are set up and solved using the Method of Moments. The equivalent magnetic currents in each layer interact with currents in the adjacent layers only, thereby resulting in a "chained-block-banded" matrix. Excitation is provided through ports defined at each pair of pads, or between a pad and nearby ground. These ports are located only on the top and the bottom layers of the PCB where the circuit components and IC pins are mounted. This formulation requires the computation of the MoM matrix only once per frequency for any number of ports. Further, the solution for only those unknown equivalent magnetic currents around the port regions is required to obtain the N-port impedance parameter characterization of the PCB. Consequently, a memory efficient block matrix solution process can be used to solve problems of large size for a given memory. Realistic PCB example is given to illustrate the validity of this approach.

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